Predictive Yield Modeling of VLSIC’s

Dennis J. Ciplickas and Xiaolei Li
PDF Solutions, Inc., San Jose, CA, USA

Andrzej J. Strojwas
Dept. of Electrical and Computer Engineering
Carnegie Mellon University, Pittsburgh, PA, USA

2000 Symposium on VLSI Technology
Statistical Metrology Workshop
June 11, 2000
Outline

- Motivation, Objectives and Approach
- Defect Detection and Characterization
- Yield Impact Estimation
- Applications
- Conclusion
Accurate quantification of yield issues allows comprehensive yield improvement planning

Predictive yield models provide one avenue for quantifying yield loss
Motivation (2)

100 chips manufactured

30 shipped to customer

70 rejected

400 MHz parts 2 chips
350 MHz parts 13 chips
300 MHz parts 15 chips

Gross functional failures
44 chips

Unrepairable cache
14 chips

Speed <300 MHz
10 chips

All others
2 chips

Errors in quantification can lead to mis-estimation of systematic failure mechanisms

Unobservable systematic and random - 2 chips

Unobservable systematic and random - 6 chips

45% of $t_{clock}$ is intrinsic RC interconnect delay

55% of $t_{clock}$ is dependent on active device performance and capacitance

Errors in quantification can lead to mis-estimation of systematic failure mechanisms.
Motivation (3)

- Yield loss mechanisms difficult to identify from sort data alone

- Empirical yield modeling methods insufficient for root cause identification
  - not necessarily predictive (is today’s solution valid tomorrow?)

- Methods based purely on inline data do not account for design-related yield sensitivities

- Predictive defect limited yield modeling enables accurate separation and quantification of mechanisms
  - can quantify by design block, defect type, process layer, etc.
  - each distinct electrical failure signatures modeled as a “micro-yield event”
Objectives

- **Determine target product yields**
  - Determine defect rates required to achieve product target yields
  - establish whether or not targets are realistic

- **Given a target or existing defect rate in the fab, determine the expected yield for a given product**
  - quantify systematic component of yield loss (yield gap analysis)
  - determine realistic product yield expectations

- **Quantification of yield loss contribution of each module or attribute**
  - rank problem modules or attributes
  - prioritize resources
  - determine yield gain expected if particular problem is fixed

- **Quantify lack of visibility of certain modules**
  - determine usefulness of developing new characterization vehicles
Summary of Approach

A modeling-based approach is a powerful tool for quantifying yield issues.
Outline

- Motivation Objectives and Approach
- Defect Detection and Characterization
- Yield Impact Estimation
- Applications
- Conclusion
Methods for Defect Detection and Characterization

- Inline inspection
- Electrical Defect Characterization
- Memory Bitmap Analysis
- Binsort/Datalog Analysis
Inline Defect Inspection

- **Inspection methods**
  - bright field (KLA 213x)
  - dark field (Surfscan 7xxx/AlTxx, Orbot WFxxx)

- **Review and classification**
  - SEM vs. optical review
  - ADC

- **Characterization**
  - Defect filtering
  - Size distribution analysis (only possible with bright field data)
  - Killer potential/Yield impact analysis
Inline Data Based DSD Model Fitting Task Flow

Raw KLA213X/KLA255x data

Filter by:
- Classification = shorts-related
- No cluster

- Very important to filter/smooth data for compatibility with yield model

Fit model for $x > x_f$

Evaluate model for $x > x_0$
Defect Filtering

- Include defect classifications related to shorts
  - particles
  - planar shorts
  - any type of extra material

- Discard other defect classifications
  - missing material/open defect (build separate model)
  - missing via
  - corrosion
  - clusters (build separate model)
  - etc.

- If partial review, must be careful to calibrate false defect rate using full review experiment
Defect Size Distribution Modeling

\[ DSD(r) = D_0 f(x) \frac{k}{x^p} \]

\[ x = \sqrt{XY} \]
Critical Area Concepts

- Critical Area, CA(x), is the area of the chip on which a defect of size x would cause a failure

Example: Line Shorts

Example: Critical Area Curve for Shorts
Critical Area Concepts: Comb Example (2)

Defect of diameter $2ls+lw$ causes at least 2 lines to short wherever it falls in the structure. $CA(x) = \text{Area of comb}$

Defect of diameter $> 2ls+lw$ causes at least 2 lines to short wherever it falls in the structure. $CA(x) = \text{Area of comb}$

$L*(ls+lw)n = \text{Area of Comb}$

Note the linear trend in $CA(x)$ due to regular comb structure.
Yield Event Prediction

\[ Y_{\text{event}_i} = \exp \left( -\int_{x_0}^{\infty} \text{CA}_{\text{event}_i}(x) \text{DSD}_l(x) \, dx \right) \]
Yield Impact vs. Defect Size
Outline

- Motivation Objectives and Approach

- Defect Detection and Characterization
  - Inline Inspection
  - Electrical Detection
  - Memory Bitmap Analysis

- Yield Impact Estimation

- Applications

- Conclusion
Electrical Defect Detection and Characterization

- Build CV
- Specify Process Flow
- Electrical Test
- Failure rate Extraction

- Mimic product patterns and pattern distributions
- Keep wafer state consistent with full flow
- Consider test time during design phase
- D0, p, Df, lambda
Typical Metal/Poly Planar Layer Short Flow CV

~22mm

Linewidth characterization
Systematic open/short yield characterization
Random defect characterization
Nest Test Structure for DSD Extraction

Same total critical area as large comb, but possible to calculate size of defect
Nest Test Structure - Concept

- 2-line shorts
- 3-line shorts
- N-line shorts

Bar chart showing the count of lines shorted:

- Count: 35
- Number of lines shorted: 2, 3, 4, 5, 6

Diagram illustrating the concept with labeled sections.
Nest Test Structure - Ideal Critical Area

Critical Area

Defect Size

2-line shorts

3-line shorts

4-line shorts

>4-lines shorted
Nest Test Structure - Actual Critical Area

Practical implementation of NEST idea requires advanced layout analysis for accurate defect size characterization.
Nest DSD Model Fitting Task Flow

- Raw E-Test data
- Filter data by wafer position and design rule of structure
- Derive failures from parametric values
- Nest structure Critical Area
- Fit D0,p parameters
Metal Defect Size Distribution Example Results

\[ \lambda = 1.69, \ p = 2.23 \]

Using multiple nests below, above and at design rule can expose process marginalities

Observed Lambda
Predicted Lambda
Contact, Via Hole Opens Yield Modeling

- Likelihood of a particle defect causing hole open is low
- Hole opens typically caused by randomly occurring systematic issues
- Estimate hole fault rate directly from test structures such as chains

\[ \lambda = \text{faults/via} \]
Example Via Short Flow CV

Via chain and single-via kelvin test structures are constructed in various configurations which mimic product layout attributes.
Hole Open Fail Rate Model Fitting Task Flow

1. Raw E-Test data
2. Filter data by wafer position and design rule of structure
3. Derive failures from parametric values
4. Number of holes in Via Chain
5. Fit $\lambda$ parameter
Example Via CV Results

Via resistance/yield dependent on metal neighborhood

Can use lambda vs. misalign for yield prediction
Electrical Defect Detection Sampling Considerations

- A trade-off exists between the test structure size and the accuracy of the fail rate calculations.
- As the test structure size decreases, more wafers are required to calculate the fail rate calculations with statistical confidence.

![Trade-off between test structure size and accuracy](image)

- Fixed fail rate
- Fixed die per wafer

Must use sufficient sampling size when calculating the failure rates.
Outline

- Motivation, Objectives and Approach

- Defect Detection and Characterization
  - Inline Inspection
  - Electrical Detection
  - Memory Bitmap Analysis

- Yield Impact Estimation

- Applications

- Conclusion
### Memory Bitmap Analysis

#### Goals

- Map Failed Bit Map Codes (Failure Modes) to the most likely defect mechanisms
- Failure Modes defined as *Yield Micro-events* in our Yield Impact Evaluation
- Pareto of defect mechanisms (per layer and defect type) evaluated using critical area and DSD
- separation of defects into two groups: in the memory array and outside of array (sense amp, decoders, datalines)

#### Applications

- root cause analysis
- aid to analytical Failure Analysis (deprocessing, FIB SEM)
- hit rate estimate for in-line detected defects
## Defect Detection and Characterization Summary

<table>
<thead>
<tr>
<th>Method</th>
<th>Pros</th>
<th>Cons</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inline inspection</td>
<td>Leverages product wafers already in fab</td>
<td>Throughput/TAT</td>
</tr>
<tr>
<td></td>
<td>Excellent defect localization</td>
<td>Sensitivity can be poor</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Killer potential not always clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Systematic failures not always observable</td>
</tr>
<tr>
<td>Electrical CV</td>
<td>Good observability systematic defects</td>
<td>Requires engineering wafers</td>
</tr>
<tr>
<td></td>
<td>Good observability random defects</td>
<td>Fault localization can be difficult</td>
</tr>
<tr>
<td></td>
<td>Killer potential often obvious</td>
<td>Root cause not clear</td>
</tr>
<tr>
<td></td>
<td>Turnaround time</td>
<td></td>
</tr>
<tr>
<td>Memory Bitmap</td>
<td>Excellent fault localization</td>
<td>Throughput/TAT</td>
</tr>
<tr>
<td></td>
<td>Good root cause identification</td>
<td>Poor observability of random logic faults</td>
</tr>
<tr>
<td></td>
<td>Killer potential is obvious</td>
<td>Requires full flow processing</td>
</tr>
<tr>
<td>Datalog Binmap</td>
<td>Killer potential is obvious</td>
<td>Fault localization poor</td>
</tr>
<tr>
<td></td>
<td>Captures all failure modes</td>
<td>Root cause usually not clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Requires full flow processing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Huge cost</td>
</tr>
</tbody>
</table>
Outline

- Motivation, Objectives and Approach
- Defect Detection and Characterization
- Yield Impact Estimation
- Applications
- Conclusion
Building The Overall Yield Impact Prediction

Product

block A  block B  block C

Yield Impact Table

Process

AA short
Poly short/open
Contact open
Metal1 short
Via open
Metal2 short
The PDF Yield Impact Table

- Example table for 2 level metal logic chip with embedded SRAM:

<table>
<thead>
<tr>
<th></th>
<th>poly</th>
<th>contact</th>
<th>metal1</th>
<th>via</th>
<th>metal2</th>
<th>Total across chip layers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic</td>
<td>$Y_{\text{Logic,poly}}$</td>
<td>$Y_{\text{Logic,contact}}$</td>
<td>$Y_{\text{Logic,metal1}}$</td>
<td>$Y_{\text{Logic,via}}$</td>
<td>$Y_{\text{Logic,metal2}}$</td>
<td>$Y_{\text{Logic}}$</td>
</tr>
<tr>
<td>SRAM</td>
<td>$Y_{\text{SRAM,poly}}$</td>
<td>$Y_{\text{SRAM,contact}}$</td>
<td>$Y_{\text{SRAM,metal1}}$</td>
<td>$Y_{\text{SRAM,via}}$</td>
<td>$Y_{\text{SRAM,metal2}}$</td>
<td>$Y_{\text{SRAM}}$</td>
</tr>
<tr>
<td>Total across chip blocks</td>
<td>$Y_{\text{poly}}$</td>
<td>$Y_{\text{contact}}$</td>
<td>$Y_{\text{metal1}}$</td>
<td>$Y_{\text{via}}$</td>
<td>$Y_{\text{metal2}}$</td>
<td>$Y_{\text{chip}}$</td>
</tr>
</tbody>
</table>

Yield of poly layer in SRAM

Yield of layer computed by taking product down column of all block yields

Yield of poly layer computed by taking product down column of all block yields
Redundant Yield Modeling

- Repaired yield prediction is easily handled by yield impact table paradigm

- Critical areas for each micro-event are treated as separate “blocks” in layout

- Each event receives a separate column or row in yield impact matrix

- If event can be repaired, cell in yield impact table treated as 100% yield
Example Micro-event Critical Areas

- Micro-event critical areas are disjoint

<table>
<thead>
<tr>
<th>Event Categorization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd,i0</td>
</tr>
<tr>
<td>bitbar,i1</td>
</tr>
<tr>
<td>word,GND</td>
</tr>
<tr>
<td>i0,bit</td>
</tr>
<tr>
<td>i1,i0</td>
</tr>
<tr>
<td>bit,word</td>
</tr>
<tr>
<td>i1,word</td>
</tr>
<tr>
<td>i0,bit,word</td>
</tr>
<tr>
<td>i1,bitbar,word</td>
</tr>
<tr>
<td>Vdd,i0,i1</td>
</tr>
<tr>
<td>Vdd,i1</td>
</tr>
<tr>
<td>i0,word</td>
</tr>
<tr>
<td>bitbar,word</td>
</tr>
</tbody>
</table>
Example Micro-event Critical Area Curves

![Graph showing normalized critical area vs. defect size for two layers: Layer 1 and Layer 2. The graph illustrates two events, Event 1 and Event 2, and their corresponding critical area distributions.]
Redundant Yield Model Formulation

Yield Impact Prediction

Memory block

- 2 column short
- 3 column short
- >3 column short
- 2 rows short
- Other shorts
- Missing cell contact

Repairable Events

Unrepairable Events

Repairable yield impact prediction

Virgin yield impact prediction

Logic block A

Logic block B
### Micro-event Yield Impact Matrix

#### Event Yields:

<table>
<thead>
<tr>
<th>LAYER/EVENT</th>
<th>1bit</th>
<th>2bit</th>
<th>nword</th>
<th>2word</th>
<th>blk1</th>
<th>blk2</th>
<th>nbl</th>
<th>2bl</th>
<th>nbita</th>
<th>nbitb</th>
<th>cross</th>
<th>other</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poly1</td>
<td>96.8%</td>
<td>99.8%</td>
<td>99.8%</td>
<td>99.4%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>98.7%</td>
</tr>
<tr>
<td>Poly2</td>
<td>88.0%</td>
<td>99.3%</td>
<td></td>
<td>95.7%</td>
<td>96.9%</td>
<td>99.3%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>99.3%</td>
<td>79.5%</td>
</tr>
<tr>
<td>Poly3</td>
<td>61.2%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>95.8%</td>
<td>92.6%</td>
<td>98.5%</td>
</tr>
<tr>
<td>Metal</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>53.5%</td>
</tr>
<tr>
<td>Virgin Core</td>
<td>85.2%</td>
<td>60.7%</td>
<td>95.6%</td>
<td>92.4%</td>
<td>95.7%</td>
<td>96.9%</td>
<td>99.3%</td>
<td></td>
<td>95.8%</td>
<td>92.6%</td>
<td>98.7%</td>
<td>96.6%</td>
<td>35.4%</td>
</tr>
<tr>
<td>C-BL</td>
<td>7.1%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>7.1%</td>
</tr>
<tr>
<td>C-BIT</td>
<td>39.1%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>39.1%</td>
</tr>
<tr>
<td>Virgin Core</td>
<td>33.3%</td>
<td>4.3%</td>
<td>95.6%</td>
<td>92.4%</td>
<td>95.7%</td>
<td>96.9%</td>
<td>99.3%</td>
<td>95.8%</td>
<td>92.6%</td>
<td>98.7%</td>
<td>96.6%</td>
<td>1.0%</td>
<td></td>
</tr>
<tr>
<td>Repaired Core</td>
<td>repair</td>
<td>repair</td>
<td>repair</td>
<td>repair</td>
<td>repair</td>
<td>repair</td>
<td>repair</td>
<td>repair</td>
<td>repair</td>
<td>repair</td>
<td>repair</td>
<td>repair</td>
<td>repair</td>
</tr>
</tbody>
</table>

#### Event Fail Frequency (1-Yield):

<table>
<thead>
<tr>
<th>LAYER/EVENT</th>
<th>1bit</th>
<th>2bit</th>
<th>nword</th>
<th>2word</th>
<th>blk1</th>
<th>blk2</th>
<th>nbl</th>
<th>2bl</th>
<th>nbita</th>
<th>nbitb</th>
<th>cross</th>
<th>other</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poly1</td>
<td>3.2%</td>
<td>0.2%</td>
<td>0.2%</td>
<td>0.6%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.3%</td>
<td>3.4%</td>
</tr>
<tr>
<td>Poly2</td>
<td>12.0%</td>
<td>0.7%</td>
<td></td>
<td>4.3%</td>
<td>3.1%</td>
<td>0.7%</td>
<td>0.7%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.7%</td>
<td>4.2%</td>
</tr>
<tr>
<td>Poly3</td>
<td>38.8%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.5%</td>
<td>7.4%</td>
</tr>
<tr>
<td>Metal</td>
<td></td>
<td></td>
<td></td>
<td>4.2%</td>
<td>7.0%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.0%</td>
</tr>
<tr>
<td>Virgin Core</td>
<td>14.8%</td>
<td>39.3%</td>
<td>4.4%</td>
<td>7.6%</td>
<td>4.3%</td>
<td>3.1%</td>
<td>0.7%</td>
<td>0.7%</td>
<td>4.2%</td>
<td>7.4%</td>
<td>1.3%</td>
<td>3.4%</td>
<td>64.6%</td>
</tr>
<tr>
<td>C-BL</td>
<td>92.9%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C-BIT</td>
<td>60.9%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Virgin Core</td>
<td>66.7%</td>
<td>95.7%</td>
<td>4.4%</td>
<td>7.6%</td>
<td>4.3%</td>
<td>3.1%</td>
<td>0.7%</td>
<td>0.7%</td>
<td>4.2%</td>
<td>7.4%</td>
<td>1.3%</td>
<td>3.4%</td>
<td>99.0%</td>
</tr>
<tr>
<td>Repaired Core</td>
<td>repair</td>
<td>repair</td>
<td>repair</td>
<td>repair</td>
<td>repair</td>
<td>repair</td>
<td>repair</td>
<td>repair</td>
<td>repair</td>
<td>repair</td>
<td>repair</td>
<td>repair</td>
<td>repair</td>
</tr>
</tbody>
</table>
Yield Model Forms and Definitions

- If defects occur uniformly across wafer/die, can use simple Poisson Model:
  
  \( Y = e^{-\text{faults/chip}} \) in general
  
  \( Y = e^{-D_0 \times Ac(p)} \) for critical area-based defects (poly, metal layers)
  
  \( Y = e^{-\lambda \times N} \) for counted defects (contacts, vias)

  where
  
  \( D_0 = \text{defects/cm}^2; \ Ac(p) = \int_{x_0}^{\infty} CA(x) \frac{k}{x^p} dx \)
  
  \( \lambda = \text{fails/count}; \ N = \# \text{ of counts} \)

- If defect distribution is not uniform, should use other yield models
  
  - Modified Poisson, Negative Binomial, Murphy, Bose-Einstein, Seeds
Outline

- Motivation, Objectives and Approach
- Defect Detection and Characterization
- Yield Impact Estimation
- Applications
- Conclusion
Applications of Predictive Yield Models

- Yield impact estimation for Embedded DRAM chip
- Yield gap analysis for high performance logic with embedded memory
- Yield prediction for FLASH memory redundancy performance
  - ASMC 1998
Yield Impact Estimation for Embedded DRAM Chip

The logic and DRAM blocks, and the core and periphery within DRAM blocks are treated separately in yield impact table.
Yield Impact Table for eDRAM Chip

<table>
<thead>
<tr>
<th>Layers / Blocks</th>
<th>Unrepaired Core</th>
<th>Repaired Core</th>
<th>Unrepaired Periphery</th>
<th>Repaired Periphery</th>
<th>DRAM Unrepaired Virgin</th>
<th>DRAM Repaired</th>
<th>LOGIC</th>
<th>Total Virgin Chip Yield</th>
<th>Total Repaired Chip Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poly1</td>
<td>88.58%</td>
<td>99.53%</td>
<td>94.46%</td>
<td>97.30%</td>
<td>83.67%</td>
<td>96.84%</td>
<td>92.25%</td>
<td>77.19%</td>
<td>89.34%</td>
</tr>
<tr>
<td>Poly2</td>
<td>77.60%</td>
<td>98.89%</td>
<td>100.00%</td>
<td>100.00%</td>
<td>81.86%</td>
<td>100.00%</td>
<td>100.00%</td>
<td>77.60%</td>
<td>98.89%</td>
</tr>
<tr>
<td>Poly3</td>
<td>87.36%</td>
<td>99.47%</td>
<td>100.00%</td>
<td>100.00%</td>
<td>91.38%</td>
<td>97.30%</td>
<td>100.00%</td>
<td>81.36%</td>
<td>99.47%</td>
</tr>
<tr>
<td>Metal1</td>
<td>100.00%</td>
<td>100.00%</td>
<td>93.05%</td>
<td>89.04%</td>
<td>93.05%</td>
<td>97.30%</td>
<td>82.18%</td>
<td>73.18%</td>
<td>76.47%</td>
</tr>
<tr>
<td>Metal2</td>
<td>100.00%</td>
<td>100.00%</td>
<td>85.56%</td>
<td>85.56%</td>
<td>87.75%</td>
<td>89.43%</td>
<td>89.43%</td>
<td>76.52%</td>
<td>76.52%</td>
</tr>
<tr>
<td>Metal3</td>
<td>100.00%</td>
<td>100.00%</td>
<td>94.46%</td>
<td>94.46%</td>
<td>94.46%</td>
<td>89.43%</td>
<td>89.43%</td>
<td>81.10%</td>
<td>81.10%</td>
</tr>
<tr>
<td>Metal4</td>
<td>100.00%</td>
<td>100.00%</td>
<td>97.39%</td>
<td>97.39%</td>
<td>97.39%</td>
<td>89.43%</td>
<td>89.43%</td>
<td>93.15%</td>
<td>93.15%</td>
</tr>
<tr>
<td>Metal5</td>
<td>100.00%</td>
<td>100.00%</td>
<td>97.39%</td>
<td>97.39%</td>
<td>97.39%</td>
<td>89.43%</td>
<td>89.43%</td>
<td>99.02%</td>
<td>99.02%</td>
</tr>
<tr>
<td>Shorts Total</td>
<td>55.93%</td>
<td>97.90%</td>
<td>66.21%</td>
<td>71.27%</td>
<td>37.03%</td>
<td>69.77%</td>
<td>55.13%</td>
<td>20.41%</td>
<td>38.47%</td>
</tr>
<tr>
<td>C-N+AA</td>
<td>100.00%</td>
<td>100.00%</td>
<td>97.90%</td>
<td>97.90%</td>
<td>97.90%</td>
<td>94.01%</td>
<td>94.01%</td>
<td>92.03%</td>
<td>92.03%</td>
</tr>
<tr>
<td>C-P+AA</td>
<td>100.00%</td>
<td>100.00%</td>
<td>98.80%</td>
<td>98.80%</td>
<td>98.80%</td>
<td>98.80%</td>
<td>98.80%</td>
<td>93.59%</td>
<td>92.46%</td>
</tr>
<tr>
<td>C-POLY</td>
<td>100.00%</td>
<td>100.00%</td>
<td>96.57%</td>
<td>96.57%</td>
<td>96.57%</td>
<td>95.92%</td>
<td>95.92%</td>
<td>92.63%</td>
<td>92.63%</td>
</tr>
<tr>
<td>Via12</td>
<td>100.00%</td>
<td>100.00%</td>
<td>98.68%</td>
<td>98.68%</td>
<td>98.68%</td>
<td>95.38%</td>
<td>95.38%</td>
<td>94.12%</td>
<td>94.12%</td>
</tr>
<tr>
<td>Via23</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Via34</td>
<td>100.00%</td>
<td>100.00%</td>
<td>99.98%</td>
<td>99.98%</td>
<td>99.98%</td>
<td>100.00%</td>
<td>100.00%</td>
<td>99.98%</td>
<td>99.98%</td>
</tr>
<tr>
<td>Via45</td>
<td>100.00%</td>
<td>100.00%</td>
<td>99.98%</td>
<td>99.98%</td>
<td>99.98%</td>
<td>100.00%</td>
<td>100.00%</td>
<td>99.98%</td>
<td>99.98%</td>
</tr>
<tr>
<td>C-BL</td>
<td>38.29%</td>
<td>100.00%</td>
<td>100.00%</td>
<td>100.00%</td>
<td>100.00%</td>
<td>100.00%</td>
<td>100.00%</td>
<td>100.00%</td>
<td>100.00%</td>
</tr>
<tr>
<td>C-WL</td>
<td>61.88%</td>
<td>100.00%</td>
<td>100.00%</td>
<td>100.00%</td>
<td>100.00%</td>
<td>100.00%</td>
<td>100.00%</td>
<td>100.00%</td>
<td>100.00%</td>
</tr>
<tr>
<td>C-BIT</td>
<td>61.88%</td>
<td>100.00%</td>
<td>100.00%</td>
<td>100.00%</td>
<td>100.00%</td>
<td>100.00%</td>
<td>100.00%</td>
<td>100.00%</td>
<td>100.00%</td>
</tr>
<tr>
<td>Opens Total</td>
<td>14.66%</td>
<td>100.00%</td>
<td>91.91%</td>
<td>91.91%</td>
<td>91.91%</td>
<td>78.49%</td>
<td>78.49%</td>
<td>10.58%</td>
<td>72.14%</td>
</tr>
<tr>
<td>Total</td>
<td>8.20%</td>
<td>97.90%</td>
<td>60.85%</td>
<td>65.50%</td>
<td>4.99%</td>
<td>64.12%</td>
<td>43.28%</td>
<td>2.16%</td>
<td>27.75%</td>
</tr>
</tbody>
</table>

Low unrepaired yield... but most defects repairable

Big Sensitivity to Metal1

Predicted Repaired DRAM Yield better than Logic Yield Block

Overall Yield strong Function of Metal1 and Via12 Logic Yield
Yield Impact Table for eDRAM Chip (cont’d)

Predicted Yields can further be broken down into individual logic blocks yields...

<table>
<thead>
<tr>
<th>Layers/Contacts</th>
<th>D0 Block A</th>
<th>Block B</th>
<th>Block C</th>
<th>Block D</th>
<th>Block E</th>
<th>Block F</th>
<th>Block G</th>
<th>Block H</th>
<th>Block I</th>
<th>Block J</th>
<th>Block K</th>
<th>Other</th>
<th>Total Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polly1</td>
<td>D0_P1</td>
<td>99.9%</td>
<td>99.9%</td>
<td>99.9%</td>
<td>100.0%</td>
<td>99.9%</td>
<td>99.9%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>98.0%</td>
</tr>
<tr>
<td>Metal1</td>
<td>D0_M1</td>
<td>99.5%</td>
<td>99.9%</td>
<td>99.9%</td>
<td>100.0%</td>
<td>99.9%</td>
<td>99.8%</td>
<td>99.8%</td>
<td>100.0%</td>
<td>99.9%</td>
<td>99.9%</td>
<td>100.0%</td>
<td>99.9%</td>
</tr>
<tr>
<td>Metal2</td>
<td>D0_M2</td>
<td>99.8%</td>
<td>99.9%</td>
<td>99.9%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>99.9%</td>
<td>99.9%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>99.9%</td>
</tr>
<tr>
<td>Metal3</td>
<td>D0_M3</td>
<td>99.5%</td>
<td>99.9%</td>
<td>99.9%</td>
<td>100.0%</td>
<td>99.9%</td>
<td>99.9%</td>
<td>99.9%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>99.7%</td>
</tr>
<tr>
<td>Metal4</td>
<td>D0_M4</td>
<td>99.8%</td>
<td>99.7%</td>
<td>99.9%</td>
<td>100.0%</td>
<td>99.9%</td>
<td>99.8%</td>
<td>98.8%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>99.9%</td>
</tr>
<tr>
<td>Shorts Total</td>
<td>λ (fails/1e9)</td>
<td>99%</td>
<td>99%</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
<td>99%</td>
<td>100%</td>
<td>98%</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
<td>97%</td>
</tr>
<tr>
<td>C-N+AA</td>
<td>λ_N+AA</td>
<td>94.9%</td>
<td>96.6%</td>
<td>97.9%</td>
<td>99.1%</td>
<td>98.7%</td>
<td>97.1%</td>
<td>98.0%</td>
<td>97.9%</td>
<td>99.3%</td>
<td>99.4%</td>
<td>97.9%</td>
<td>99.2%</td>
</tr>
<tr>
<td>C-P+AA</td>
<td>λ_P+AA</td>
<td>93.5%</td>
<td>97.5%</td>
<td>97.1%</td>
<td>98.8%</td>
<td>98.3%</td>
<td>96.3%</td>
<td>97.3%</td>
<td>97.4%</td>
<td>99.0%</td>
<td>99.2%</td>
<td>97.3%</td>
<td>98.7%</td>
</tr>
<tr>
<td>C-Poly1</td>
<td>λ_Poly</td>
<td>95.8%</td>
<td>96.9%</td>
<td>98.4%</td>
<td>99.4%</td>
<td>99.2%</td>
<td>97.8%</td>
<td>98.4%</td>
<td>98.6%</td>
<td>99.1%</td>
<td>98.9%</td>
<td>98.5%</td>
<td>99.0%</td>
</tr>
<tr>
<td>Via12</td>
<td>λ_v12</td>
<td>99.7%</td>
<td>99.8%</td>
<td>99.9%</td>
<td>100.0%</td>
<td>99.9%</td>
<td>99.9%</td>
<td>99.9%</td>
<td>99.9%</td>
<td>99.9%</td>
<td>99.9%</td>
<td>99.9%</td>
<td>100.0%</td>
</tr>
<tr>
<td>Via23</td>
<td>λ_v23</td>
<td>99%</td>
<td>99.9%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>99.9%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
</tr>
<tr>
<td>Via34</td>
<td>λ_v34</td>
<td>99%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
<td>100.0%</td>
</tr>
<tr>
<td>Opens+Shorts Total</td>
<td></td>
<td>91%</td>
<td>93%</td>
<td>97%</td>
<td>96%</td>
<td>91%</td>
<td>94%</td>
<td>94%</td>
<td>97%</td>
<td>97%</td>
<td>94%</td>
<td>97%</td>
<td>97%</td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td>90%</td>
<td>93%</td>
<td>97%</td>
<td>96%</td>
<td>91%</td>
<td>93%</td>
<td>92%</td>
<td>97%</td>
<td>97%</td>
<td>93%</td>
<td>94%</td>
<td>42%</td>
</tr>
</tbody>
</table>

No apparent block-specific M1 problem because all logic blocks are equally sensitive to M1.

Block A is most sensitive to Contact Failures.
Conclusions From eDRAM Yield Prediction

- Logic yield loss more significant than DRAM yield loss, after accounting for repair

- Metal1 significantly affects all logic blocks

- Logic block A is sensitive to Contact yield and may benefit from re-design with redundant contacts
Yield Gap Analysis

- Electrical CV Data
  - Nominal
  - $D_0$, $p$ and $\lambda$
  - $D_0$, $p$ and $\lambda$ Variation
  - Yield Prediction
    - Nominal
    - $3\sigma$

- Product Design
- Layout
- Wafer Sort
  - Test Data
  - Actual Yield
    - Nominal
    - $3\sigma$

Compare
Yield Gap Analysis Result

Mean value variation in DRAM and Logic yields due to METAL and CONTACT module defects

0% mean shift

Systematic logic yield gap with parametric signature

Metal module defects, contact module defects and logic yield gap were target areas of diagnosis work
Outline

- Motivation, Objectives and Approach
- Defect Detection and Characterization
- Yield Impact Estimation
- Applications
- Conclusion
Conclusions

- **Determine target product yields**
  - Determine defect rates required to achieve product target yields
  - establish whether or not targets are realistic

- **Given a target or existing defect rate in the fab, determine the expected yield for a given product**
  - quantify systematic component of yield loss (yield gap analysis)
  - determine realistic product yield expectations

- **Quantification of yield loss contribution of each module or attribute**
  - rank problem modules or attributes
  - prioritize resources
  - determine yield gain expected if particular problem is fixed

- **Quantify lack of visibility of certain modules**
  - determine usefulness of developing new characterization vehicles
Acknowledgements

- We would like to acknowledge our colleagues at PDF Solutions for their constructive help in building the methods and results described here.

- In particular, we would like to acknowledge Kimon Michaels, Sherry Lee and Rakesh Vallishayee for their in depth contributions to this work.